What Is Claimed Is:

1. A semiconductor integrated circuit comprising:

an output circuit comprising plural output MOSFETs connected in parallel;

a first control means that, from among the plural output MOSFETs, selects the number of output MOSFETS to be turned on to control output impedance; and

a second control means that controls slew rate by controlling a drive signal of the output MOSFETs turned on.

2. The semiconductor integrated circuit according to claim 1,

wherein the output MOSFETs connected in parallel are divided into plural groups,

the output MOSFETs of the plural groups are respectively divided into plural subgroups,

the first control means forms a signal for selecting the plural groups,

the second control means controls the timing of driving output MOSFETs of the plural subgroups, and

correspondingly to data to be outputted, plural output MOSFETs comprising one or plural groups selected by the first control means are turned on correspondingly to a drive timing formed by the second control means.

3. The semiconductor integrated circuit according to claim 2,

output impedance controlled by the first control means is set so as to match characteristic impedance of transmission lines through which signals conveyed by the output MOSFETs are transmitted.

4. The semiconductor integrated circuit according to claim 3,

wherein, correspondingly to each of the plural MOSFETs, an output prebuffer for driving it is disposed, and

the output prebuffer is activated by the data to be outputted and a selection signal formed by the first control means, and the rise time of a drive signal conveyed to the output MOSFET is changed by a control signal formed by the second control means.

5. The semiconductor integrated circuit according to claim 4,

wherein a resistance element is connected in series with each of the output MOSFETs.

6. The semiconductor integrated circuit according to claim 5,

wherein a resistance value of the resistance element is almost equal to or greater than a resistance value of the on-state output MOSFET.

7. The semiconductor integrated circuit according to claim 6,

wherein the circuit is configured in which impedance ratios of output MOSFETs making up the subgroups are almost equal among the plural groups, to prevent slew rate control from being influenced by a result of output impedance control.

8. The semiconductor integrated circuit according to claim 6,

wherein the output MOSFET comprises a first MOSFET of first conduction type that forms an output signal of a level corresponding to a power voltage side, and a second MOSFET of second conduction type that forms an output signal of a level corresponding to ground potential side of the circuit, and

the first MOSFET and the second MOSFET are respectively provided with the output prebuffers.

9. The semiconductor integrated circuit according to claim 8,

wherein the first MOSFET, the second MOSFET, and the resistance element can be connected by one straight wiring to form a layout of a basic structure, and

two or more of the basic structures comprising the first MOSFET, the second MOSFET, and the resistance element are disposed in parallel in a stripe form in a direction orthogonal to the wiring.

10. The semiconductor integrated circuit according to claim 9,

wherein, in the plural layouts of the basic structures disposed in parallel, stripe units having lower impedance have larger MOSFET size in a direction of extension of the wiring and smaller resistance size in a direction of extension of the wiring, while stripe units having higher impedance have smaller MOSFET size in a direction of extension of the wiring and larger resistance size in a direction of extension of the wiring, and the difference between the stripe units of the plural basic structures is made small.

11. The semiconductor integrated circuit according to claim 10,

wherein the stripe units further include an antistatic diode connected correspondingly to the straight wirings.

12. The semiconductor integrated circuit according to claim 6,

wherein the first control means includes a resistance element connected to an external terminal, and forms a signal for selecting the MOSFETs so as to produce output impedance closest to a resistance value of the resistance element connected to the external terminal.

13. The semiconductor integrated circuit according to claim 12,

wherein the output circuit is divided into plural groups, which are interspersed on a semiconductor board,

the first control means is disposed on the semiconductor board,

the selection signal formed by the first control means is conveyed to a latch circuit disposed for each of the groups, and

the latch circuit captures the selection signal correspondingly to a clock pulse, and conveys the captured selection signal to a corresponding output circuit.

14. A semiconductor integrated circuit comprising:

an input circuit that receives input signals supplied from an external terminal;

a terminal circuit that is connected to the external terminal and includes plural MOSFETs connected in parallel; and

a third control means that controls the number of the plural MOSFETs to be turned on to control a resistance value of terminal resistance.

15. The semiconductor integrated circuit according to claim 14,

wherein the MOSFET comprises a third MOSFET of first conduction type disposed at power voltage side and a fourth MOSFET of second conduction type disposed at a ground potential side of the circuit.

16. The semiconductor integrated circuit according to claim 15,

wherein the third MOSFET and the fourth MOSFET can be connected by one straight wiring to form a layout of a basic structure, and

two or more of the basic structures comprising the third MOSFET and the fourth MOSFET are disposed in parallel in a stripe form in a direction orthogonal to the wiring.

17. The semiconductor integrated circuit according to claim 16,

wherein the stripe units further include an antistatic diode connected correspondingly to the straight wirings.

18. The semiconductor integrated circuit according to claim 16,

wherein the third control means includes a resistance element connected to an external terminal, and forms a signal for selecting the third MOSFET and the fourth MOSFET so as to produce a resistance value closest to a resistance value of the resistance element connected to the external terminal.

19. The semiconductor integrated circuit according to claim 18,

wherein the third MOSFET and the fourth MOSFET respectively comprise plural pieces having an on-state resistance value of a binary weight, and are selectively turned on by a selection signal of binary code formed by the third control means.

20. The semiconductor integrated circuit according to claim 19,

wherein each of the third MOSFET and the fourth MOSFET comprises first plural pieces whose on-state resistance values have weights of low-order bits of the binary code, and second plural pieces each having the same on-state resistance value assigned to high-order bits of the binary code, and

low-order bits of the selection signal of binary code formed by the third control means are used to select corresponding MOSFETs of the first plural pieces from among the plural pieces of the third MOSFET and the fourth MOSFET, and code corresponding to the high-order bits is supplied to a decoder circuit and used to select corresponding MOSFETs of the second plural pieces.

21. The semiconductor integrated circuit according to claim 19,

wherein the third control means comprises:

a resistance element connected to the external terminal;

a first circuit that forms a binary control signal for a first replica circuit so as to bring partial output of power voltage formed by the first replica circuit of the third MOSFET and a midpoint voltage of the power voltage into the nearest to each other; and

a second circuit, controlled by the binary control signal formed by the first circuit, that forms a binary control signal

for the third replica circuit so as to bring partial output of power voltage formed by a second replica circuit corresponding to the third MOSFET and a third replica circuit of the fourth MOSFET and a midpoint voltage of the power voltage into the nearest to each other, wherein the binary control signal of the first circuit is conveyed as a selection signal of the third MOSFET, and the binary control signal of the second circuit is conveyed as a selection signal of the fourth MOSFET.

22. The semiconductor integrated circuit according to claim 21,

wherein the binary control signal of the first circuit and the binary control signal of the second circuit are respectively conveyed to shift circuits, and corrected selection signals are respectively conveyed to the third MOSFET and the fourth MOSFET.

23. A semiconductor integrated circuit comprising:

an output circuit which includes plural output MOSFETs connected in parallel and whose output node is connected to an external terminal;

a first control means that selects the number of the plural output MOSFETs to be turned on to control output impedance;

a second control means that controls slew rate by controlling a drive signal of the output MOSFETs to be turned on;

an input circuit that receives input signals supplied from the external terminal;

a terminal circuit including plural MOSFETs connected in parallel; and

a third control means that controls the number of the plural MOSFETs to be turned on to control a resistance value of terminal resistance.

24. The semiconductor integrated circuit according to claim 23,

wherein the third control means turns off all plural MOSFETs controlled by the output circuit when brought into operation.

25. The semiconductor integrated circuit according to claim 24,

wherein the output MOSFET comprises a first MOSFET of first conduction type that forms an output signal of a level corresponding to a power voltage side, and a second MOSFET of second conduction type that forms an output signal of a level corresponding to ground potential side of the circuit, and a resistance element is connected in series with each of the first MOSFET and the second MOSFET, and

the MOSFETs making up the terminal circuit include a third MOSFET of first conduction type disposed at power voltage side and a fourth MOSFET of second conduction type disposed at ground potential side of the circuit.

26. The semiconductor integrated circuit according to claim 25,

wherein the first MOSFET, the second MOSFET, and the resistance element, and the third MOSFET and the fourth MOSFET can be connected by one straight wiring to form a layout of a basic structure, and

two or more of the basic structures comprising the first MOSFET, the second MOSFET, and the resistance element, and the third MOSFET and the fourth MOSFET are disposed in parallel in a stripe form in a direction orthogonal to the wiring.

27. The semiconductor integrated circuit according to claim 26,

wherein the first control means includes a first resistance element connected to a first external element, and forms a signal for selecting the plural first MOSFETs and second MOSFETs so as to produce output impedance closest to a resistance value of the first resistance element connected to the first external terminal, and

the third control means includes a second resistance element connected to a second external terminal and forms a signal for selecting the plural third MOSFETs and fourth MOSFETs so as to produce output impedance closest to a resistance value of the second resistance element connected to the second external terminal.